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EXAMINER	
LAROSE, COLIN M	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/449,022	GOLDBERG ET AL.	
	Examiner	Art Unit	
	Colin M. LaRose	2627	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-47* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Arguments and Amendments

1. Applicant's amendments and arguments filed 28 December 2005, have been entered and made of record.

Response to Amendments, Arguments, and Affidavit

2. Applicant has amended independent claims 1 and 39 to denote that a "first processor" and a "selected processor," respectively, are operative to substantially simultaneously analyze substantially all of the image portions distributed thereto. This newly-added limitation renders the claims indefinite because it requires an image portion to be "substantially simultaneously" analyzed, rather than e.g. parallel processors to simultaneously analyze the portions.

It is unclear how an image portion can be "substantially simultaneously" analyzed by itself. "Simultaneous" refers to two events occurring at the same time or concurrently, but the claims require an image portion to be "simultaneously" analyzed without referencing the other "simultaneous" event.

3. Applicant has amended independent claims 11, 18 and 34 to denote that "each of the at least two processors" or "each slave processor" is operative to substantially simultaneously analyze substantially all of the image portions distributed thereto.

Forslund is considered to fairly disclose such a feature insofar as Forslund's processors analyze image portions simultaneously in parallel. In addition, simultaneous analysis occurs in Forslund's increased parallelism whereby the processors are divided into two processors for a divide-and-conquer scheme, such as shown in figure 7B.

4. Applicant has amended independent claim 24 to denote that the selected processor analyzes "substantially all" of its respective image portions, and similar limitations appear in independent claims 1, 11, 18, 34, and 39.

Applicant asserts that Forslund does not disclose this feature because Forslund employs "pipeline" processing, whereas the disclosed invention employs "patch" processing. After considering the Affidavit of Mr. Lawrence R. Miller and the corresponding remarks by Applicant's representative, the Examiner appreciates the differences between both types of processing.

However, it does not appear that such differences are reflected in the claims. The claims, as amended, merely call for the processors to analyze "substantially all" of their respective image portions. It is clear from Forslund's disclosure that an entire image is to be analyzed – wherein a first processor processes a first portion, and a second processor processes a second portion, as shown in figure 7B. That is, substantially all of the two image portions shown in figure 7B of Forslund are in fact analyzed by corresponding processors. As such, it is unclear how the assertion that Forslund employs pipelined processing negatives the fact that the entire first and second image portions are analyzed by the processors. It appears that the issue of "patch" vs. "pipelined" processing centers around how many pixels are processed contiguously within each processor and thus how many pixels at a time are delivered to the respective processors. But Forslund's utilization of pipelined processing does not mean that the respective processors are incapable of analyzing "substantially all of the image portions" – it only means that a limited number of pixels are delivered to and processed by the processors within a given cycle.

Claim Objections

5. The following sections of 37 CFR §1.75(a) and (d)(1) are the basis of the following objection:

> (a) The specification must conclude with a claim particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention or discovery.
>
> (d)(1) The claim or claims must conform to the invention as set forth in the remainder of the specification and the terms and phrases used in the claims must find clear support or antecedent basis in the description so that the meaning of the terms in the claims may be ascertainable by reference to the description.

6. Claims 1-10 and 39-47 are objected to under 37 CFR §1.75(a) and (d)(1) as failing to particularly point out and distinctly claim the subject matter that the applicant regards as the invention.

Applicant has amended independent claims 1 and 39 to denote that a "first processor" and a "selected processor," respectively, are operative to substantially simultaneously analyze substantially all of the image portions distributed thereto. This newly-added limitation renders the claims indefinite because it requires an image portion to be "substantially simultaneously" analyzed, rather than e.g. parallel processors to simultaneously analyze two different portions.

It is unclear how an image portion can be "substantially simultaneously" analyzed by itself. "Simultaneous" refers to two events occurring at the same time or concurrently, but the claims require an image portion to be "simultaneously" analyzed without referencing the other "simultaneous" event.

Appropriate correction and/or clarification is required.

Allowable Subject Matter

7. The claim limitation of the processors analyzing "substantially all" of their respective image portions is not considered to distinguish from Forslund. However, it is clear that Forslund processes the image data in a "pipeline" manner whereas the present invention utilizes a "patch-based" method (see e.g. Miller's Affidavit dated 7/29/05).

The affidavit identifies the primary difference between Forslund's pipeline method and the present invention's patch-based method as follows:

Forslund delivers one line of image data to a processor at a time – the line corresponding to 16 pixels on consecutive raster lines – and then the processor processes the line of 16. In a next time slot, a second set of 16 pixels are delivered and processed, and so on. Therefore, no more than one line of pixel data is delivered and stored in the processors at any given time. See paragraph 4 of the affidavit.

In contrast, the present invention's patch-based method delivers rectangular patches to the processors, where each patch is stored and processed by the processor as a unit. See paragraph 4 of the affidavit.

This distinction between Forslund and the present invention, if sufficiently embodied in the claims, would distinguish the present invention from Forslund and render the claims allowable. In particular, the Specification on p. 14-15, teaches each processor being "coupled to or integrated with one or more memory devices" that hold the image data portion corresponding to a rectangular patch of the sample. Examiner believes that such a feature of the claimed

invention distinguishes from Forslund insofar as Forslund's processors are not "coupled to or integrated with" memory devices that store corresponding rectangular patches.

In other words, Forslund does not provide each processor with a separate memory area for storing a "rectangular" patch of image data that is to be analyzed by the processor. At best, Forslund teaches that each processor has memory sufficient to hold one line of image data in accordance with a pipeline image data processing method.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1, 3-9, 18, 22-25, 27-30, 34, 37-39, and 41-44 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 5,659,630 by Forslund.

Regarding claim 1, Forslund discloses an apparatus for inspecting a plurality of image portions of at least a region of a sample for defects, the apparatus comprising:

a plurality of processors (elements 67, figure 5) arranged to receive (from registration 66) and analyze at least one of the image portions, the processors being arranged to operate in parallel and being configurable (column 13, lines 40-42) to implement one or more algorithms selected from a plurality of different algorithms for analyzing the image portions (column 13, lines 38-46: the channels (processors 67, figure 5) are modified to inspect different products

having different specifications; the algorithms are used to determine defective areas indicative of shorts, opens, pad voids, etc.); and

a registration system (element 66, figure 5) arranged to receive image data (i.e. data captured from camera 64, and image from database 62), select at least a first processor (e.g. "shorts" processor) for receiving a first image portion of the image data and not a second image portion, select at least a second processor (e.g. "opens" processor) for receiving the second image portion of the image data and not the first image portion, and output the first image portion to the first processor and the second image portion to the second processor (column 6, lines 20-22: the registration 66 distributes all image portions (i.e. pixel blocks, figure 7) to all processors; therefore, the first processor receives a first portion, and the second processor receives a second portion), wherein the first image portion and the second image portion are different rectangular shaped image portions that each has a width that comprises a plurality of pixels and a length that comprises a plurality of pixels (see figure 7B, where the image is divided into two rectangular portions),

wherein the first processor is then operable to implement the one or more first algorithms to analyze substantially all of the first image portion to determine whether the analyzed first image portion has a defect and the second processor is then operable to implement the one ore more second algorithms to analyze substantially all of the second image portion to determine whether the analyzed second image portion has a defect (i.e. Forslund's processors are operable to analyze the entirety of each respective image portion) .

Similar features are present in independent claims 18, 24, 34, and 39, which are all taught by Forslund.

Regarding claim 2, Forslund discloses the system of figure 5 is further arranged to divide the aligned image data into a plurality of image portions (figure 7). Forslund does not expressly disclose that the registration system 66 divides the image, however, it is apparent that this is the case since the dividing occurs before transmission to the processors and after alignment of the images received from blocks 62 and 65, and both said transmission and said alignment are performed by the registration system 66.

Regarding claim 3, Forslund discloses the first processor is arranged to receive a first reference image portion (i.e. reference data from database 62, figure 5, or alternatively, reference image derived from camera 64) corresponding to the first image portion and to compare the first image portion to the first reference image portion ("reference image" and "image" data are aligned by registration 66, and the shorts processor compares the two to detect defects), and the second processor ("opens" processor) is arranged to receive a second reference image portion corresponding to the second image portion and to compare the second image portion to the second reference image portion (registration 66 distributes all aligned "reference image" and "image" portions to all of the processors 67 for comparison), and

wherein determining whether the analyzed first image portion has a defect is based on the comparison between the first image portion and the first reference image portion and determining whether the analyzed second image portion has a defect is based on the comparison between the second image portion and the second reference image portion (see e.g. figure 5 for reference-to-sample comparison) .

Regarding claims 4 and 5, Forslund discloses the first image portion differs from the second image portion (figure 7B: the portions correspond to the different portions of the image).

Regarding claim 6, Forslund discloses at least a part of the first image portion is identical to at least part of the second image portion (column 6, line 59: "overlap" among windows).

Regarding claim 7, Forslund discloses the first processor is configured with a different algorithm for analyzing the first image portion than the second processor ("shorts" detects short circuits, "opens" detects open circuits).

Regarding claim 8, Forslund discloses the first reference image portion is derived from a corresponding portion of the sample (image of sample captured by camera 64).

Regarding claim 9, Forslund discloses the first reference image portion is derived from a file used to design the sample (alternatively, the first reference image is from the CAD database 60, figure 5).

Regarding claim 24, Forslund discloses a method for analyzing image data obtained from a sample using a plurality of processors, comprising the acts of:

receiving image data from an inspection system that generates the image data from a sample (image data generated from camera 64, figure 5);

dividing the image data into a plurality of image portions that correspond to various portions of the sample (figure 7);

outputting each image portion to a selected processor, at least some of the image portions going to different processors (all image portions are driven to multiple defect processors 67, figure 5), each processor being configurable (column 13, lines 40-42) to implement one or more algorithms (e.g. short detection, open detection, etc.) selected from a plurality of different

algorithms for analyzing the image portions to determine whether the corresponding portions of the sample are defective;

analyzing substantially all of each image portion for defects within the selected processor based on the selected one or more algorithms for such selected processor to determine whether the corresponding portion of the same has a defect (e.g. analyze all of each portion for open and short circuits); and

outputting and combining results from each processor such that defect data is compiled for the entire image data (defect data is compiled into memory 69, figure 5).

Regarding claim 25, Forslund discloses at least some of the image portions are analyzed with different algorithms ("shorts" detects short circuits, "opens" detects open circuits).

Regarding claim 27, Forslund discloses receiving reference data corresponding to each image portion (CAD data 60, figure 5).

Regarding claim 28, each image portion is analyzed by comparing each image portion to its corresponding reference data (reference and image data are aligned, and the processors 67 compare the two to detect defects).

Regarding claim 29, Forslund discloses the reference data is in form of a corresponding image portion of the sample (column 6, lines 4-9: both reference data and sample image are rasterized images).

Regarding claim 30, Forslund discloses the reference data is in form of design data that is used to construct the sample (reference data is CAD data from database 60, figure 5).

Regarding claim 39, Forslund discloses a computer readable medium containing program instructions for inspecting a sample having a plurality of fine patterns thereon, and processing data resulting from the inspection, the computer readable medium comprising computer codes corresponding to the steps of claim 24, as well as a computer readable medium for storing the computer readable codes (each block in figure 5 has codes stored in hardware or software).

Regarding claim 41, see the explanation for claim 27.

Regarding claim 42, see the explanation for claim 28.

Regarding claim 43, see the explanation for claim 29.

Regarding claim 44, see the explanation for claim 30.

Regarding claim 18, Forslund discloses a method of inspecting a sample having a plurality of fine patterns thereon, and processing data resulting from the inspection, comprising:

a) receiving data (from blocks 62 and 65, figure 5) derived from the inspection in a multiprocessor system, the system comprising a master processor (element 66, figure 5) and a plurality of slave processors (elements 67, figure 5);

b) dividing the data into groups using the master processor (column 6, lines 20-22: registration 66 drives the image data to the defect detectors 67, and column 6, lines 50-54: data is divided into groups; it is not clear whether registration 66 divides the data, but it would have been apparent to one skilled in the art that dividing the data occurs by the registration 66 before the data is driven to the detectors 67) and sending a different group to each one of the slave processors, each data group corresponding to information derived from a portion of the sample, wherein the first image portion and the second image portion are different rectangular shaped

image portions that each has a width that comprises a plurality of pixels and a length that comprises a plurality of pixels (see figure 7B, where the image is divided into two rectangular portions), wherein each slave processor (67, figure 5) is configurable (column 13, lines 40-42) to implement one or more algorithms selected from a plurality of different algorithms for substantially simultaneously analyzing substantially all of its received data group to determine whether the corresponding portion of the sample is defective (algorithms used by the slave processors 67 determine presence of defects such as shorts, opens, etc. in portions of the entire sample);

c) selecting one more algorithms from the plurality of different algorithms for each slave processor and configuring each slave processor with the selected algorithm(s) for each slave processor (i.e. an algorithm – open detection, short detection, etc. – is selected for each slave processor 67)

d) processing the data groups with the slave processors based on the selected algorithm(s) for each processor (defect detectors 67 process the groups to find defects); and

e) deriving defect information regarding the sample and the fine patterns from the combined data (columns 9-10: "Shorts Detection" and "Opens Detection" sections provide details for deriving defect information from the combined data).

Regarding claim 22, Forslund discloses the data groups are processed using an algorithm which compares data derived from differing regions of the sample (figure 7: differing window regions are processed using the comparison algorithms of defect detectors 67, figure 5).

Regarding claim 23, Forslund discloses the data groups are processed using an algorithm which compares data derived from a portion of the sample with data derived from a file used to design the sample (image of sample from camera 64 is compared with design data from CAD database 60 during defect detection performed by processors 67).

Regarding claim 34, Forslund discloses a computer readable medium (figure 5) containing program instructions for inspecting a sample having a plurality of fine patterns thereon, and processing data resulting from the inspection, the computer readable medium comprising computer codes corresponding to the steps of claim 18, as well as a computer readable medium for storing the computer readable codes (each block in figure 5 has codes stored in hardware or software).

Regarding claim 37, see the explanation for claim 22.

Regarding claim 38, see the explanation for claim 23.

Claim Rejections - 35 USC § 103

10. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

11. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Forslund and U.S. Patent 6,081,659 by Garza et al. ("Garza").

Regarding claim 10, Forslund discloses the first processor is arranged to receive a first reference data portion (from CAD database 60) that characterizes a pattern in the sample that the first image portion corresponds to, and the post processor 61 is arranged to render the first

reference data portion to a first reference image portion and the first processor is arranged to compare the first reference image portion to the first image portion (reference and image data are aligned, and output to processor 73, which compares the two to detect defects, and the first processor 73 renders the reference image portion in figure 13).

Forslund does not disclose the first processor renders the reference data portion to a first reference image, since Forslund's system renders the reference data portion prior to distribution of the image portions to the first processor.

Garza discloses an inspection system that renders reference data to a reference image (step 212, figure 7) and compares the reference image to an image of a sample (step 218, figure 7). Both of the rendering and comparing is carried out by the simulator 140, figure 4. The simulator comprises a single processor 148 that executes the stored computer instructions for rendering and software instructions for comparing (column 7, lines 17-26).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Forslund by Garza in order to render the first reference data portion using the first processor, since Garza shows that a single processor performs both the functions of rendering and comparing, thus eliminating the need for separate processors.

12. Claims 11-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Forslund and U.S. Patent 5,357,632 by Pian et al. ("Pian").

Regarding claim 11, Forslund discloses an apparatus for inspecting a plurality of image portions of at least a region of a sample, the apparatus comprising:

a distributor (registration 66 and buffers 70,72, figure 9) arranged to receive the image portions; and

a plurality of processors (73-76, figure 9) that are arranged into a plurality of subgroups ("shorts detection" subgroup, "opens detection" subgroup, "pad void detection" subgroup) that are each coupled to an associated distributor (figure 9: each of the subgroups are associated to the distributor), each processor being configurable (column 13, lines 40-42) to implement one or more algorithms (short detection, open detection, etc.) selected from a plurality of different algorithms for analyzing the image portions to determine whether the corresponding regions of the sample are defective, the distributor being configurable to output selected image portions to its associated subgroup of processors (elements 70 and 72 output the selected portions from the registration 66 to the associated subgroups), at least two of the processors being arranged to analyze at [least] two of the image portions in parallel (elements 73-75 analyze all image portions in parallel),

wherein the image portions are different rectangular shaped image portions that each has a width that comprises a plurality of pixels and a length that comprises a plurality of pixels (see e.g. figure 7B),

wherein each of the at least two processors are operable to implement its selected one or more algorithms to analyze substantially all of each of its image portions to determine whether the analyzed each image portion has a defect (i.e. Forslund's processors are operable to analyze the entirety of each respective image portion).

Forslund does not disclose a plurality of distributors arranged to receive the image portions.

Pian discloses a dynamic task allocation system in which a plurality of distributors (112, figure 3) are each configured to output partitioned blocks of data (column 1, lines 61-68) to an associated arithmetic processor.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Forslund by Pian to include a plurality of distributors, each outputting selected image portions to a defect processor subgroup, since Pian shows that a system employing, inter alia, a plurality of distributors improves data flow and task allocation for parallel arithmetic processors (column 2, lines 50-57).

Furthermore, utilizing a plurality of distributors in lieu of a single distributor does not bear patentable significance since the addition of extra distributors does not produce new or unexpected results. As would have been obvious to one skilled in the art, a plurality of distributors is able to distribute more data than a single distributor. Other than this obvious advantage, the specification does not disclose any new or unexpected results due to the inclusion of more distributors. Therefore, modifying Forslund to include multiple distributors was considered to be within the level of ordinary skill in the art at the time the invention was made. See *In re Harza*, 274 F.2d 669, 124 USPQ 378 (CCPA 1960).

Regarding claim 12, Pian does not disclose the distributors are arranged in a daisy chain configuration such that a first distributor receives the image portions and outputs one or more of the image portions to a second distributor. However, arranging distributors in a daisy chain fashion to distribute data to processing elements was known at the time the invention was made, as were advantages of utilizing the daisy chain configuration. Official notice taken.

Regarding claim 13, Pian discloses each subgroup of processors 114, figure 3 includes a supervisor processor 122 that is coupled with an associated one of the distributors (supervisor 122 is coupled to each one of the distributors 112) so as to receive the selected image portions from the associated distributor (the processors 114 receive partitioned data from the distributors 112 via communication lines 116), wherein each supervisor processor is configurable to distribute the selected image portions to selected processors within its associated subgroup (the supervisor 122 distributes the data portions to the processors 114 via the distributors 112).

It would have been obvious to one of ordinary skill in the art at the time of the invention to further modify Forslund by Pian to achieve the claimed invention since Pian discloses the above arrangement of a supervisor, processor subgroups, and distributors produces improved data flow and task allocation for systems that utilize parallel data processing (column 2, lines 50-57).

Regarding claim 14, Forslund discloses a first processor is arranged to receive a selected image portion and a selected reference image portion corresponding to the selected image portion and to compare the selected image portion to the selected reference image portion (reference and image data are aligned, and output to processor 73, which compares the two to detect defects).

Regarding claim 15, see the explanation for claim 10.

Regarding claim 16, see the explanation for claim 8.

Regarding claim 17, see the explanation for claim 9.

13. Claims 20 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Forslund and U.S. Patent 4,181,936 by Kober.

Regarding claim 20, Forslund discloses the system comprises a master processor, in communication with a plurality of slave processors.

Forslund is silent to the system comprising a plurality of master processors, each in communication with a plurality of slave processors, and wherein each of the master processors is in communication with a central processor, the central processor allocating data among the master processors.

Kober discloses a distributed computing system in which a data exchange processor (62, figure 1) functions as a central processor that allocates data among a plurality of computers (53,54(64),55, figure 1). Column 1, lines 58-63: the data exchange processor controls the data transfer among the individual computers.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Forslund by Kober so that Forslund's system comprises a plurality of master processors (individual computers 53,54,55 of Kober each contain Forslund's system of figure 5, which comprises master processor 66), each in communication with a plurality of slave processors (67, figure 5 of Forslund), and wherein each of the master processors is in communication with a central processor (62, figure 1 of Kober), the central processor allocating data among the master processors, since Forslund discloses utilizing a parallel processing architecture in order to process a collection of data in a reduced period of time, wherein the data is broken into subgroups and processed by different processors (column 6, lines 50-59 of Forslund), and Kober discloses utilizing a central processor controlling the flow of data to a

plurality of parallel computers reduces the data transmission time (column 2, lines 26-33 of Kober).

Regarding claim 35, see the explanation for claim 20.

14. Claims 21, 26, 36, and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Forslund and U.S. Patent 4,999,785 by Schmuter.

Regarding claim 21, Forlsund is silent to a first group of the slave processors using one or more algorithms selected to process data with high accuracy, but at a relatively slow rate, and wherein a second group of the slave processors using one or more algorithms selected to process data with a relatively low accuracy, but at a high rate.

Schmuter discloses a method for inspecting defects in a circuit board that uses a first group of slave processors to process data with low accuracy at a high rate, and a second group of slave processors to process data with a relatively high accuracy at a high rate. In reference to figure 1, inspection data is sent to a first group (7) of processors (8,9), which detects general defects of the inspection data at a coarse resolution. Any detected defects are sent to the second group (13) of processors (15,16) for an inspection of more detailed characteristics (column 3, lines 23-36). The processing of the first group is done at a coarser resolution (lower accuracy) than that of the second group, and the first group operates at a higher rate (column 5, lines 16-20: amount of time needed by the first group to detect defects is less than the time needed by the second group to evaluate the defects).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Forslund by Schmuter so that a first group of the slave processors using one or more

algorithms selected to process data with high accuracy, but at a relatively slow rate, and wherein a second group of the slave processors using one or more algorithms selected to process data with a relatively low accuracy, but at a high rate, since Scmuter discloses that this feature greatly reduces the amount of time needed to detect defects in circuit boards (column 4, lines 1-10).

Regarding claim 26, Forlsund is silent to analyzing some image portions more stringently than others.

Schmuter discloses an inspection system wherein a first group of processors (7, figure 1) detects general defects, and a second group of processors (13, figure 1) evaluates only the defects detected by the first group (column 3, lines 23-36). Therefore, the image portions containing detected defects are analyzed more stringently than those that do not have detected defects.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Forslund by Schmuter to achieve the claimed invention since Scmuter discloses that analyzing some image portions more stringently than other reduces processing time and increase throughput (column 4, lines 1-10).

Regarding claim 36, see the explanation for claim 21.

Regarding claim 40, see the explanation for claim 26.

15. Claims 31-33 and 45-47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Forslund and U.S. Patent 4,484,349 by McCubbrey.

Regarding claims 31-33, receiving control data is an inherent part of Forslund's system. As was known to one skilled in the art, control data, or computer instructions, are received, stored, and utilized at the various blocks in figure 5, which correspond to a computer

implementation of Forslund's invention. Those of skill in the art knew that any functions performed by computers must be programmed in some fashion using computer instructions (control data). Official notice taken. For example, the registration 66 receives and stores control data that specifies, inter alia, how to align two images; the segmentation block 65 receives and stores control data on how to produce a threshold image; each of the processors 67 receive and store control data that specifies an inspection algorithm; etc. If there is no control data available for a particular task, a system component is unable to perform the task. Therefore, the presence of control data for each of Forslund's computer-implemented image processing function is implicit.

Further in regards to claim 31, Forslund does not expressly disclose receiving control data that specifies how to divide and output the image portions to their selected processors.

McCubbrey discloses receiving transformation criteria values (control data) that specify how to divide the image portions, which consequently determines how the image portions are outputted (column 4, lines 22-28).

It would have been obvious to one of ordinary skill in the art at the time of the invention to receive said criteria values as control data for dividing and outputting the image portions, since Forslund discloses McCubbrey's prior art teaching on partitioning an image portion for parallel processing (column 6, line 65 of Forslund).

Further in regards to claim 32, Forslund does not expressly disclose the control data also specifies how to analyze the image portions for defects within the selected processors. However, as stated above, defect processors 67, figure 5 implicitly receive, store, and process control data specifying how to analyze image portions for defects.

Further in regards to claim 33, Forslund discloses the reference data is in form of design data that is used to construct the sample (CAD database 60, figure 5)

Forslund does not expressly disclose the control data also specifies how to render the reference data from the design data. Postprocessor 61 rasterizes (column 5, lines 63-65) the design data into the reference data format. Control data that specifies the details of the conversion is assumed to be present.

Regarding claim 45, see the explanation for claim 31.

Regarding claim 46, see the explanation for claim 32.

Regarding claim 47, see the explanation for claim 33.

16. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Forslund.

Regarding claim 19, Forslund's inspection system relates to "an inspection system for manufacturing processes and ... has particular application to the inspection of parts, such as printed circuit boards (PCBs) or cards and the like" (column 1, lines 25-30).

Forslund does not expressly disclose that the sample is selected from a group consisting of a reticle, a photomask, and a semiconductor material, device, or surface, however, methods for inspecting patterns on PCBs and semiconductors are very closely related, and one skilled in the art would have known that methods for inspecting fine patterns on PCBs can be implemented to inspect fine patterns on reticles, photomasks, and semiconductor devices with a reasonable expectation of success. Official notice taken.

Conclusion

17. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Colin M. LaRose whose telephone number is (571) 272-7423. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jingge Wu, can be reached on (571) 272-7429. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the TC 2600 Customer Service Office whose telephone number is (571) 272-2600.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CML
Group Art Unit 2627
2 March 2006

VIKKRAM BALI
PRIMARY EXAMINER